4.In each quadruples, The sub-block are placed as a matrix , like 8 column and 8 row.

5. The bus of address and Data to write or match are routed to the mid-point at each Side and then sent to the center of the chip or CAM unit.

6. The writing data are sent to the right side or left side based on the first level decoding, then sent to the particular column based on the second level decoding, then are sent to the particular sub-block based on the third level decoding.

7. only the reading out data take the data bus at different level, say, only the particular sub-block in each column will take the bus and among 8 column , only the column in which there is a reading sub-block will take the data bus.

8. On search or match case, only the highest priority hit sub-block will take the Match Address result bus on that column among the 8 sub-block, then only the highest priority hit column Will take the Match Address result bus among the 8 column.

9. The data writing can be pipe lined into multi-cycle.

10. The address decoding of data writing can be divided into multi-cycle.

11. .For Reading data, the address decoding can be divided into multi-cycle.

12. The data read out can be divided into multi-cycle.

13. the address match or search can be divided into multi-cycle.

14. the priority encoding can be divided into multi-cycle.

15. The each sub-block are independent sub-block with its own address decoding and write and read buffer as well as priority encoding.

16. Each sub-block are identical on the internal design and interface.

17. the logic interface in each column among each sub-block are identical.

18. the logic interface among each column for four quadruple are identical.